LSM320DL

Linear sensor module
3D accelerometer sensor and 2D gyroscope sensor

Preliminary data

Features

- Analog supply voltage 2.4 V to 3.6 V
- Digital supply voltage IOs, 1.8 V
- Low power mode
- Power-down mode
- 3 independent acceleration channels and 2 angular rate channels (pitch and yaw)
- ±2g/±4g/±8/±16g dynamically selectable full-scale
- ±250/±500/±2000 dps dynamically selectable full-scale
- Embedded temperature sensor
- SPI/I^2C serial interface (16-bit data output)
- Programmable interrupt generator for free-fall and motion detection
- ECOPACK® RoHS and “Green” compliant

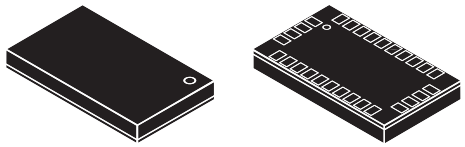
Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM320DL is a system-in-package featuring a 3D digital accelerometer and a 2D digital gyroscope.

The ST modules family uses a robust and mature manufacturing process already used for the production of micromachined accelerometers.



LGA 28L 7.5 x 4.4 x 1.1 mm

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

LSM320DL has a dynamic user selectable full-scale acceleration range of ±2*g*/±4*g*/±8/±16*g* and angular rate of ±250/±500/±2000 deg/sec.

The accelerometer and gyroscope sensors can be either activated or put in low power/power-down mode separately for application optimized power saving.

The LSM320DL is available in a plastic land grid array (LGA) package.

Several years ago ST successfully pioneered the use of this package for accelerometers. Today, ST has the widest manufacturing capability and strongest expertise in the world for production of sensors in a plastic LGA package.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packing
LSM320DL	-40 to +85	LGA 28L	Tray
LSM320DLTR			Tape and reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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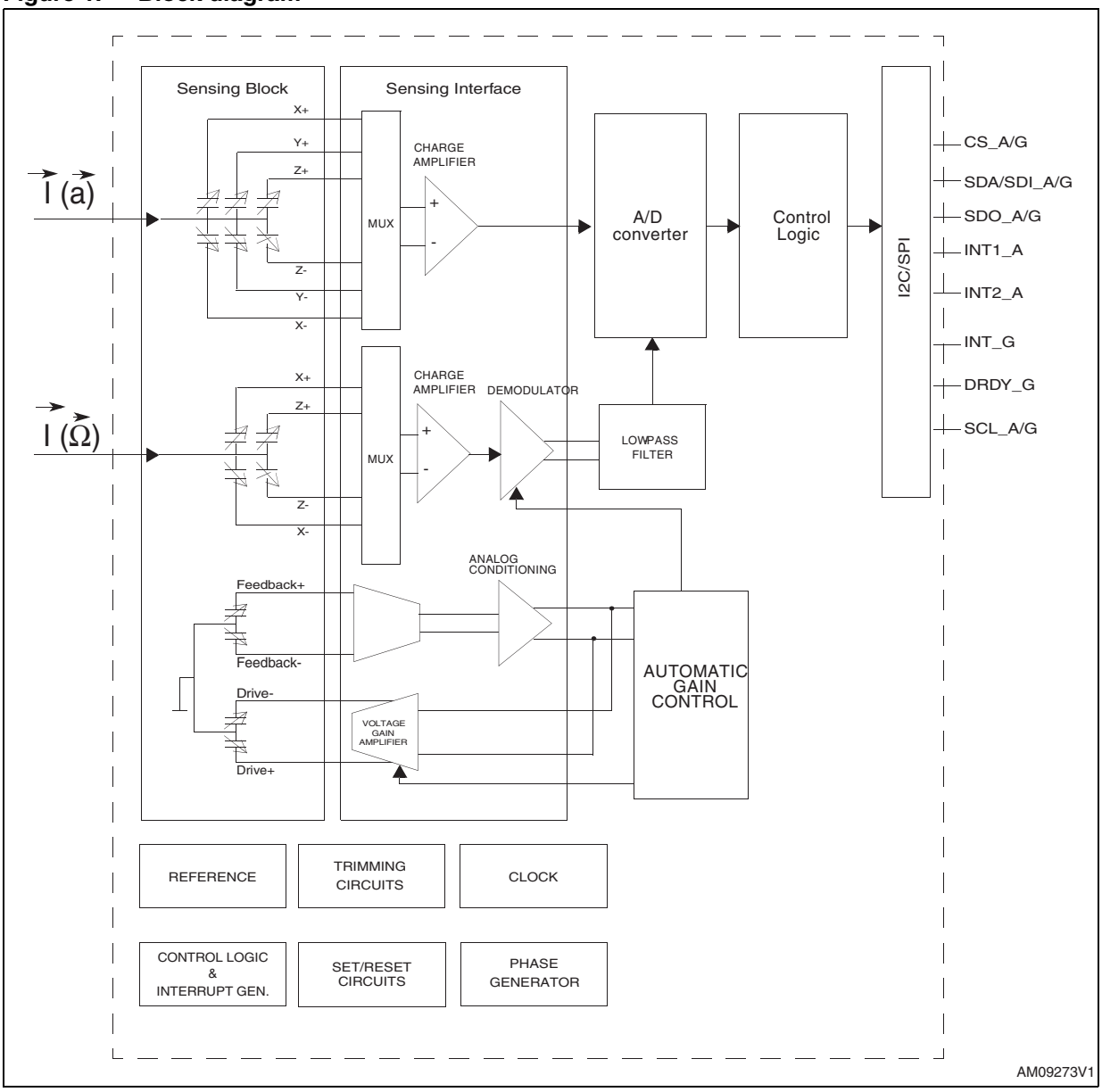
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

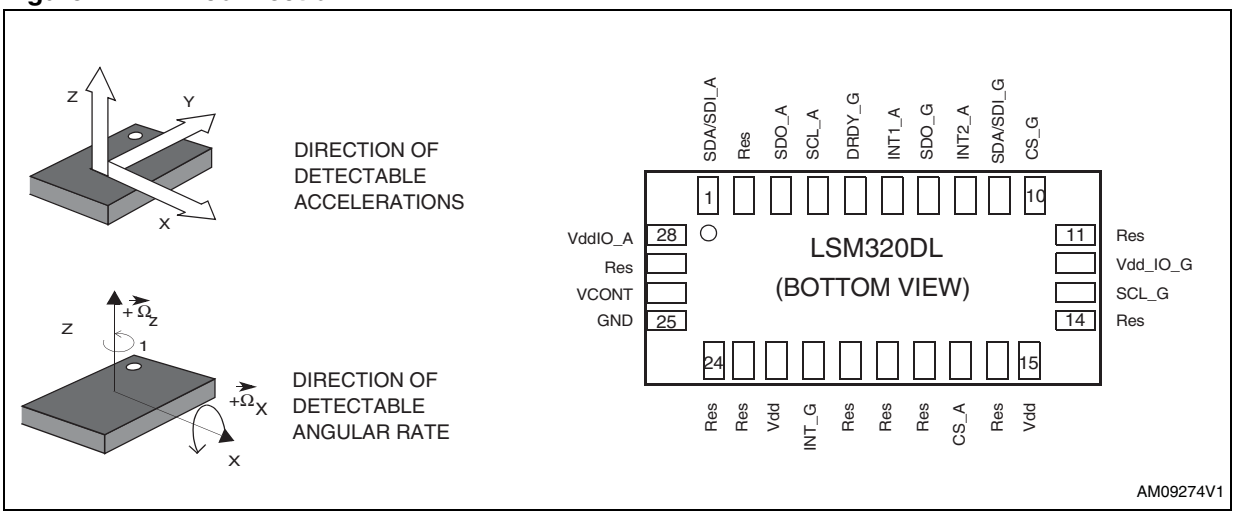


Table 2. Pin description

Pin#	Name	Function
1	SDA/SDI_A	Accelerometer: I^{2}C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
2	Res	Reserved connect to GND
3	SDO_A	Accelerometer: SPI serial data output (SDO) I^{2}C least significant bit of the device address (SA0)
4	SCL_A	Accelerometer: I^{2}C serial clock (SCL) SPI serial port clock (SPC)
5	DRDY_G	Gyroscope data ready
6	INT1_A	Accelerometer interrupt signal
7	SDO_G	Gyroscope: SPI serial data output (SDO) I^{2}C least significant bit of the device address (SA0)
8	INT2_A	Accelerometer interrupt signal
9	SDA/SDI_G	Gyroscope: I^{2}C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

Table 2. Pin description (continued)

Pin#	Name	Function
10	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
11	Res	Reserved connect to GND
12	VddIO_G	Gyroscope power supply for IO pins
13	SCL_G	Gyroscope: I^2C serial clock (SCL) SPI serial port clock (SPC)
14	Res	Reserved connect to GND
15	Vdd	Power supply
16	Res	Reserved connect to GND
17	CS_A	Accelerometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
18	Res	Reserved connect to GND
19	Res	Reserved connect to GND
20	Res	Reserved connect to GND
21	INT_G	Gyroscope interrupt signal
22	Vdd	Power supply
23	Res	Reserved connect to GND
24	Res	Reserved connect to GND
25	GND	0 V power supply
26	VCONT	PLL filter connection
27	Res	Reserved connect to GND
28	VddIO_A	Accelerometer power supply for IO pins

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]	FS bit set to 00		±2.0		*g*
		FS bit set to 01		±4.0		
		FS bit set to 10		±8.0		
		FS bit set to 11		±16.0		
G_FS	Angular rate measurement range[2]	FS bit set to 00		±250		dps
		FS bit set to 01		±500		
		FS bit set to 10		±2000		
LA_So	Linear acceleration sensitivity	FS bit set to 00		1		m*g*/digit
		FS bit set to 01		2		
		FS bit set to 10		4		
		FS bit set to 11		12		
G_So	Angular rate sensitivity	FS bit set to 00		8.75		mdps/ digit
		FS bit set to 01		17.5		
		FS bit set to 10		70		
LA_So	Linear acceleration sensitivity change vs. temperature	FS bit set to 00		±0.05		%/°C
G_So	Angular rate sensitivity change vs. temperature	From -40 to +85 °C		±2		%
LA_TyOff	Typical Zero-*g* level offset accuracy[3]	FS bit set to 00		±60		m*g*
G_TyOff	Typical zero-rate level[4]	FS bit set to 00		10		LSb
LA_TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
G_TCOff	Zero-rate level change vs. temperature	FS bit set to 00 from -40 to +85 °C		±0.03		dps/°C
An	Acceleration noise density	FS bit set to 00 Normal mode, ODR bit set to 1001		220		µ*g*/√Hz
Rn	Rate noise density	FS bit set to 00		0.03		°/s/√Hz
Top	Operating temperature range		-40		+85	°C

a. The product is factory calibrated at 3 V. The operational power supply range is from 2.4 V to 3.6 V.

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical Zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high pass filter.

2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd+0.1	V
LA_Idd	LA current consumption in normal mode	ODR = 50Hz		11		µA
		ODR = 1Hz		2		
LA_IddLowP	LA current consumption in low power mode	ODR = 50Hz		6		µA
LA_IddPdn	LA current consumption in power-down mode	T = 25°C		0.5		µA
G_Idd	AR current consumption in normal mode			6		mA
G_IddSL	Supply current in sleep mode(2)			1.5		mA
G_IddPdn	AR current consumption in power-down mode	T = 25 °C		5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T= 25 °C, unless otherwise noted.[b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

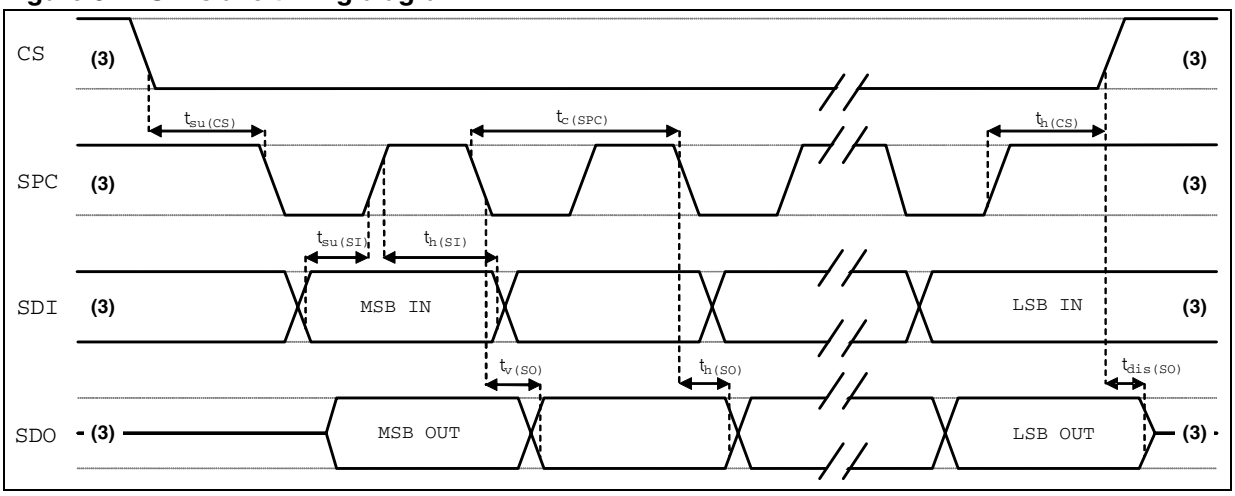
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value [1]		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	6		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	9		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram [c]



3. When no communication is on-going, data on CS, SPC, SDI, and SDO are driven by internal pull-up resistors.

c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter IC control interface

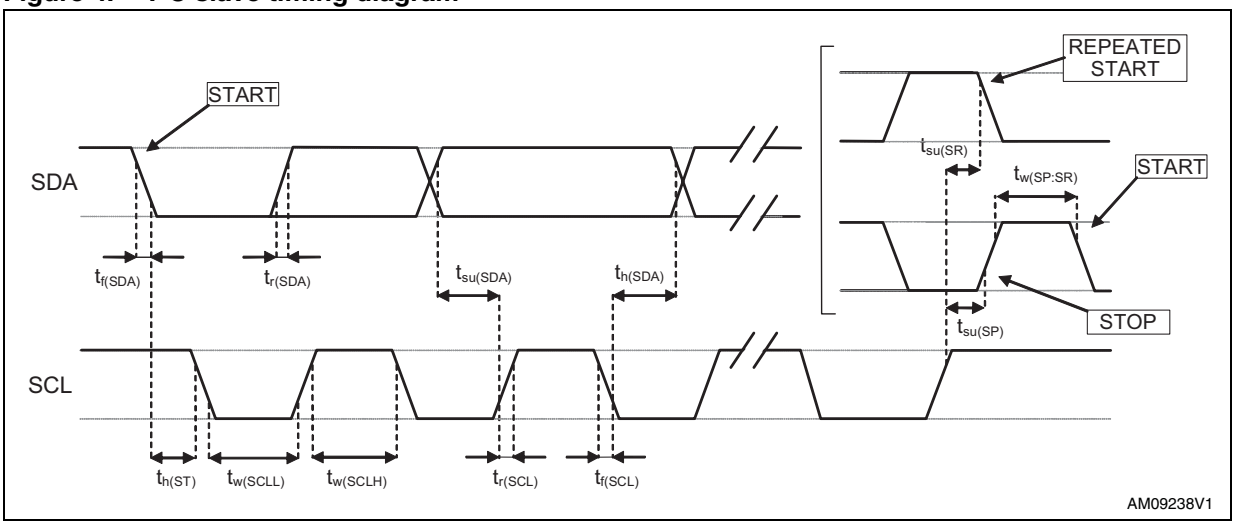
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0,01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	ns
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(SP)}$	STOP condition setup time	4		0.6		µs
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		µs

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram (d)



d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL, SDA/SDI)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

Angular rate sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and also very little over time.

2.6.2 Zero level

Linear acceleration Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in the X axis and 0 *g* in the Y axis, whereas the Z axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. The offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and also very little over time.

3 Functionality

The LSM320DL is a system-in-package featuring a 3D digital accelerometer and a 2D digital gyroscope.

The complete device includes specific sensing elements and two IC interfaces able to measure both the acceleration and angular rate applied to the module and to provide a signal to the external world through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM320DL may also be configured to generate an inertial wake-up and free-fall interrupt signal according to a programmed acceleration event along the enabled axes.

3.1 Factory calibration

The IC interface is factory calibrated for sensitivity and zero level. The trimming values are stored inside the device by a non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

4 Application hints

Figure 5. LSM320DL electrical connection

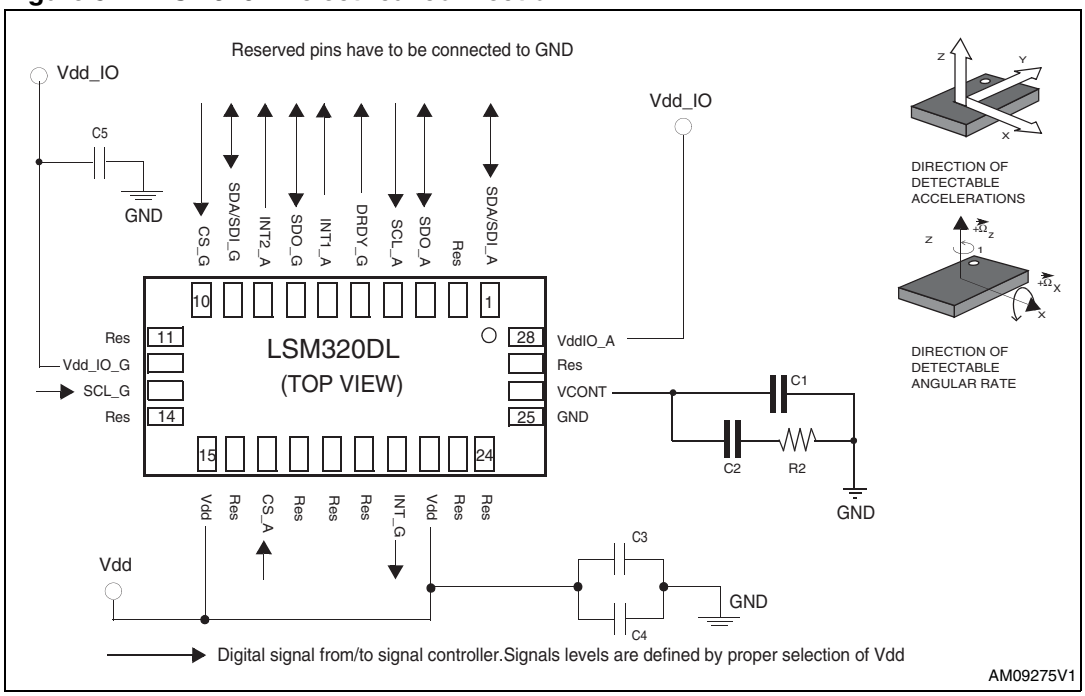


Table 9. Part list

Component	Typical value
C1	10 nF
C2	470 nF
C3	10 µF
C4	100 nF
C5	100 nF
R2	10 kOhm

4.1 External capacitors

The device core is supplied through Vdd line. Power supply decoupling capacitors (C4=100 *nF* ceramic, C3=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I^2C interface.

The functions, the threshold, and the timing of the two interrupt pins for each sensor can be completely programmed by the user though the SPI/I^2C interface.

4.2 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020D.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

5 Digital interfaces

The registers embedded inside the LSM320DL may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

To select/exploit the I^2C interface, CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS_A	Linear acceleration SPI enable Linear acceleration I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
CS_G	Angular Rate SPI enable Angular Rate I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL_A SCL_G	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI_A SDA/SDI_G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO_A SDO_G	I^2C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.1 I^2C serial interface

The LSM320DL I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM320DL behaves as a slave device and the following protocol must be adhered to. After the start condition (ST), a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/write.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can’t receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW, to force the transmitter into a wait

state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function), the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is Master Acknowledge, and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pad can be used to modify less significant bits of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (ex. address 0011001b), or else, if the SA0 pad is connected to ground, the LSb value is '0' (ex address 0011000b).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master transmits to the slave with direction unchanged. *Table 16* and *Table 17* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration address: the default (factory) 7-bit slave address is 001100xb.

Table 16. Linear acceleration SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Angular rate sensor: the default (factory) 7-bit slave address is 110100xb.

Table 17. Angular rate SAD+Read/Write patterns

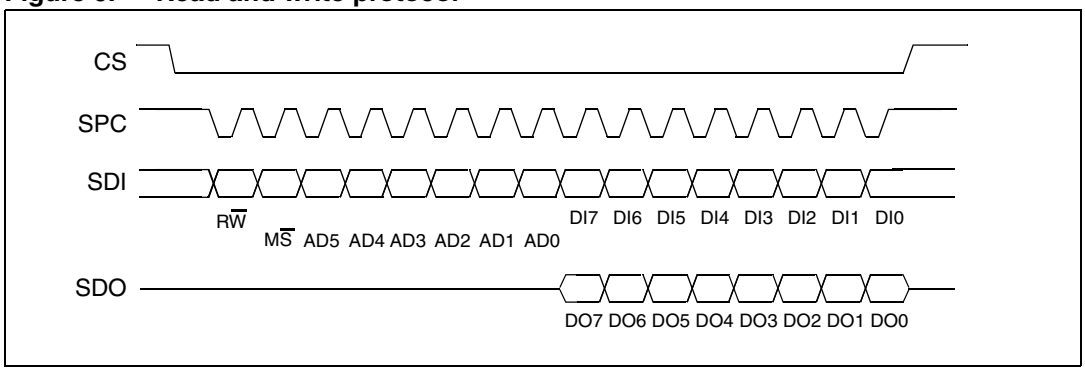
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110100	0	1	11010001 (F1h)
Write	110100	0	0	11010000 (F0h)
Read	110100	1	1	11010011 (F3h)
Write	110100	1	0	11010010 (F2h)

5.2 SPI bus interface

The LSM320DL SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI**, and **SDO**.(SPC, SDI, SD0 are common)

Figure 6. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

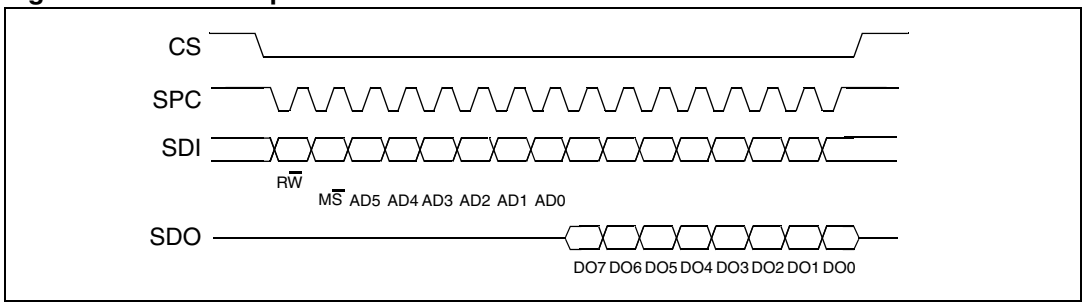
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is ‘0’, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

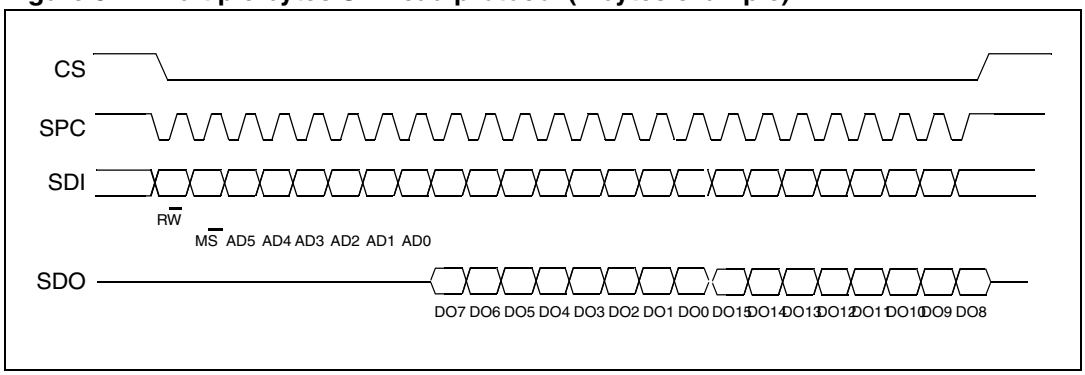
bit 1: M$\overline{S}$ bit. When 0, do not increment address, when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

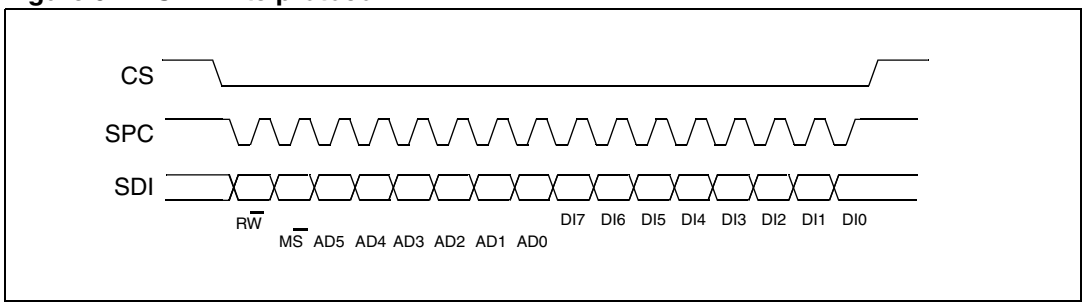
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)



5.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

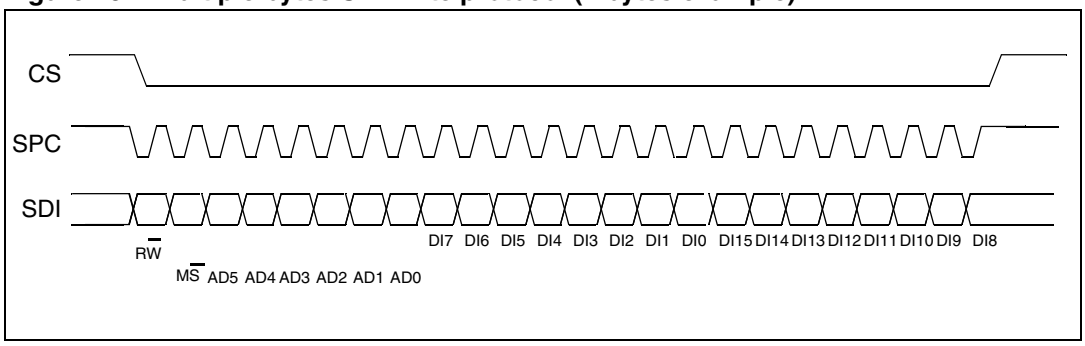
bit 1: M$\overline{S}$ bit. When 0, do not increment address, when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

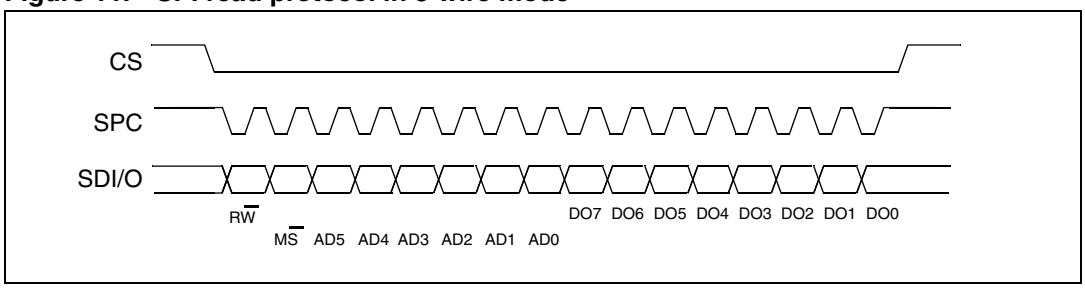
Figure 10. Multiple bytes SPI write protocol (2 bytes example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting to ‘1’ bit SIM (SPI serial interface mode selection) in CTRL_REG4.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, do not increment address, when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

6 Register mapping

Table 18 below provides a listing of the 8-bit registers embedded in the device and the related addresses:

Table 18. Register address map

Name	Slave Address	Type	Register address		Default	Comment
			Hex	Binary		
Reserved (do not modify)	001100xb		00 - 1F			Reserved
CTRL_REG1_A	001100xb	rw	20	010 0000	00000111	
CTRL_REG2_A	001100xb	rw	21	010 0001	00000000	
CTRL_REG3_A	001100xb	rw	22	010 0010	00000000	
CTRL_REG4_A	001100xb	rw	23	010 0011	00000000	
CTRL_REG5_A	001100xb	rw	24	010 0100	00000000	
CTRL_REG6_A	001100xb	rw	25	010 0101	00000000	
REFERENCE_A	001100xb	rw	26	010 0110	00000000	
STATUS_REG_A	001100xb	r	27	010 0111	00000000	
OUT_X_L_A	001100xb	r	28	010 1000	output	
OUT_X_H_A	001100xb	r	29	010 1001	output	
OUT_Y_L_A	001100xb	r	2A	010 1010	output	
OUT_Y_H_A	001100xb	r	2B	010 1011	output	
OUT_Z_L_A	001100xb	r	2C	010 1100	output	
OUT_Z_H_A	001100xb	r	2D	010 1101	output	
FIFO_CTRL_REG	001100xb	rw	2E	010 1110	00000000	
FIFO_SRC_REG	001100xb	r	2F	010 1111		
INT1_CFG_A	001100xb	rw	30	011 0000	00000000	
INT1_SOURCE_A	001100xb	r	31	011 0001	00000000	
INT1_THS_A	001100xb	rw	32	011 0010	00000000	
INT1_DURATION_A	001100xb	rw	33	011 0011	00000000	
INT2_CFG_A	001100xb	rw	34	011 0100	00000000	
INT2_SOURCE_A	001100xb	r	35	011 0101	00000000	
INT2_THS_A	001100xb	rw	36	011 0110	00000000	
INT2_DURATION_A	001100xb	rw	37	011 0111	00000000	
CLICK_CFG_A	001100xb	rw	38	011 1000	00000000	
CLICK_SRC_A	001100xb	rw	39	011 1001	00000000	
CLICK_THS_A	001100xb	rw	3A	011 1010	00000000	
TIME_LIMIT_A	001100xb	rw	3B	011 1011	00000000	

Table 18. Register address map (continued)

Name	Slave Address	Type	Register address		Default	Comment
			Hex	Binary		
TIME_LATENCY_A	001100xb	rw	3C	011 1100	00000000	
TIME_WINDOW_A	001100xb	rw	3D	011 1101	00000000	
Reserved (do not modify)	001100xb		3E-3F	-	-	Reserved
Reserved	110100xb	-	00-1E	-	-	Reserved
CTRL_REG1_G	110100xb	rw	20	010 0000	00000111	
CTRL_REG2_G	110100xb	rw	21	010 0001	00000000	
CTRL_REG3_G	110100xb	rw	22	010 0010	00000000	
CTRL_REG4_G	110100xb	rw	23	010 0011	00000000	
CTRL_REG5_G	110100xb	rw	24	010 0100	00000000	
REFERENCE_G	110100xb	rw	25	010 0101	00000000	
OUT_TEMP_G	110100xb	r	26	010 0110	output	
STATUS_REG_G	110100xb	r	27	010 0111	output	
OUT_X_L_G	110100xb	r	28	010 1000	output	
OUT_X_H_G	110100xb	r	29	010 1001	output	
Reserved	110100xb	r	2A	-	-	Reserved
Reserved	110100xb	r	2B	-	-	Reserved
OUT_Z_L_G	110100xb	r	2C	010 1100	output	
OUT_Z_H_G	110100xb	r	2D	010 1101	output	
FIFO_CTRL_REG_G	110100xb	rw	2E	010 1110	00000000	
FIFO_SRC_REG_G	110100xb	r	2F	010 1111	output	
INT1_CFG_G	110100xb	rw	30	011 0000	00000000	
INT1_SRC_G	110100xb	r	31	011 0001	output	
INT1_TSH_XH_G	110100xb	rw	32	011 0010	00000000	
INT1_TSH_XL_G	110100xb	rw	33	011 0011	00000000	
Reserved	110100xb	rw	34	-	-	Reserved
Reserved	110100xb	rw	35	-	-	Reserved
INT1_TSH_ZH_G	110100xb	rw	36	011 0110	00000000	
INT1_TSH_ZL_G	110100xb	rw	37	011 0111	00000000	
INT1_DURATION_G	110100xb	rw	38	011 1000	00000000	

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Registers description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration, angular rate and temperature data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

7.1 CTRL_REG1_A (20h)

Table 19. CTRL_REG1_A register

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

Table 20. CTRL_REG1_A description

ODR3-0	Data rate selection. Default value: 0 (0000: power-down; Others: refer to *Table 21.*, “Data rate configuration”)
LPen	Low power mode enable. Default value: 0 (0: normal mode; 1: low power mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

ODR<3:0> is used to set power mode and ODR selection. In *Table 21* all the frequencies resulting in a combination of ODR<3:0> are reported.

Table 21. Data rate configuration

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power down mode
0	0	0	1	Normal / low power mode (1 Hz)
0	0	1	0	Normal / low power mode (10 Hz)
0	0	1	1	Normal / low power mode (25 Hz)
0	1	0	0	Normal / low power mode (50 Hz)
0	1	0	1	Normal / low power mode (100 Hz)
0	1	1	0	Normal / low power mode (200 Hz)
0	1	1	1	Normal / low power mode (400 Hz)
1	0	0	0	Low power mode (1.620 kHz)
1	0	0	1	Normal (1.344 kHz) / Low Power mode (5.376 kHz)

7.2 CTRL_REG2_A (21h)

Table 22. CTRL_REG2_A register

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

Table 23. CTRL_REG2_A description

HPM1 -HPM0	High pass filter mode selection. Default value: 00 Refer to *Table 24*
HPCF2 - HPCF1	High pass filter cut-off frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPCLICK	High pass filter enabled for CLICK function. (0: filter bypassed; 1: filter enabled)
HPIS2	High pass filter enabled for AOI function on interrupt 2, (0: filter bypassed; 1: filter enabled)
HPIS1	High pass filter enabled for AOI function on interrupt 1, (0: filter bypassed; 1: filter enabled)

Table 24. High pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

7.3 CTRL_REG3_A (22h)

Table 25. CTRL_REG3_A register

I1_CLICK	I1_AOI1	0(1)	I1_DRDY1	I1_DRDY2	I1_WTM	I1_OVERRUN	--

1. This bit must be set to ‘0’ for correct operation.

Table 26. CTRL_REG3_A description

I1_CLICK	CLICK interrupt on INT1. Default value 0. (0: disable; 1: enable)
I1_AOI1	AOI1 interrupt on INT1. Default value 0. (0: disable; 1: enable)

Table 26. CTRL_REG3_A description (continued)

I1_DRDY1	DRDY1 interrupt on INT1. Default value 0. (0: disable; 1: enable)
I1_DRDY2	DRDY2 interrupt on INT1. Default value 0. (0: disable; 1: enable)
I1_WTM	FIFO Watermark interrupt on INT1. Default value 0. (0: disable; 1: enable)
I1_OVERRUN	FIFO Overrun interrupt on INT1. Default value 0. (0: disable; 1: enable)

7.4 CTRL_REG4_A (23h)

Table 27. CTRL_REG4_A register

0(1)	BLE	FS1	FS0	HR	0(1)	0(1)	SIM

1. This bit must be set to ‘0’ for correct operation.

Table 28. CTRL_REG4_A description

BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1-FS0	Full scale selection. default value: 00 (00: +/- 2G; 01: +/- 4G; 10: +/- 8G; 11: +/- 16G)
HR	High resolution output mode: default value: 0 (0: high resolution disable; 1: high resolution enable)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

7.5 CTRL_REG5_A (24h)

Table 29. CTRL_REG5_A register

BOOT	FIFO_EN	--	--	LIR_INT1	D4D_INT1	0(1)	0(1)

1. This bit must be set to ‘0’ for correct operation.

Table 30. CTRL_REG5_A description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
LIR_INT1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT1	4D enable: 4D detection is enabled on INT1 when 6D bit on INT1_CFG is set to 1.

7.6 CTRL_REG6_A (25h)

Table 31. CTRL_REG6_A register

I2_CLICKen	I2_INT1	0(1)	BOOT_I2	0(1)	--	H_LACTIVE	--

1. This bit must be set to '0' for correct operation.

Table 32. CTRL_REG6 description

I2_CLICKen	Click interrupt on INT2. Default value 0.
I2_INT1	Interrupt 1 function enabled on INT2. Default 0.
BOOT_I2	Boot on INT2.
H_LACTIVE	0: interrupt active high; 1: interrupt active low.

7.7 REFERENCE/DATACAPTURE_A (26h)

Table 33. REFERENCE_A register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 34. REFERENCE register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

7.8 STATUS_REG_A (27h)

Table 35. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 36. STATUS_REG_A register description

ZYXOR	X, Y, and Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous ones)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y, and Z axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

Table 36. STATUS_REG_A register description (continued)

ZDA	Z axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)

7.9 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed in 2's complement.

7.10 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed in 2's complement.

7.11 OUT_Z_L _A(2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed in 2's complement.

7.12 FIFO_CTRL_REG_A (2Eh)

Table 37. FIFO_CTRL_REG_A register

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

Table 38. FIFO_CTRL_REG_A register description

FM1-FM0	FIFO mode selection. Default value: 00 (see *Table 39*)
TR	Trigger selection. Default value: 0 0: trigger event linked to trigger signal on INT1 1: trigger event linked to trigger signal on INT2
FTH4:0	Default value: 0

Table 39. FIFO mode configuration

FM1	FM0	FIFO mode
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Trigger mode

7.13 FIFO_SRC_REG_A (2Fh)

Table 40. FIFO_SRC_REG_A register

WTM	OVRN_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

7.14 INT1_CFG_A (30h)

Table 41. INT1_CFG_REG_A register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 42. INT1_CFG_REG_A description

AOI	AND/OR combination of interrupt events. Default value: 0. Refer to *Table 43*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 43*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 43. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from unknown zone to known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

7.15 INT1_SRC_A (31h)

Table 44. INT1_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 45. INT1_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read only register.

Reading at this address clears the INT1_SRC IA bit (and the interrupt signal on the INT 1 pin) and allows the refreshment of data in the INT1_SRC register if the latched option is chosen.

7.16 INT1_THS_A (32h)

Table 46. INT1_THS_A register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 47. INT1_THS_A description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.17 INT1_DURATION_A (33h)

Table 48. INT1_DURATION_Aregister

0	D6	D5	D4	D3	D2	D1	D0

Table 49. INT1_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

7.18 CLICK_CFG _A (38h)

Table 50. CLICK_CFG_A register

--	--	ZD	ZS	YD	YS	XD	XS

Table 51. CLICK_CFG_A description

ZD	Enable interrupt double CLICK on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single CLICK on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double CLICK on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single CLICK on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double CLICK on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single CLICK on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

7.19 CLICK_SRC_A (39h)

Table 52. CLICK_SRC_A register

--	IA	DCLICK	SCLICK	Sign	Z	Y	X

Table 53. CLICK_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DCLICK	Double CLICK-CLICK enable. Default value: 0 (0: double CLICK-CLICK detection disable, 1: double CLICK-CLICK detection enable)
SCLICK	Single CLICK-CLICK enable. Default value: 0 (0: single CLICK-CLICK detection disable, 1: single CLICK-CLICK detection enable)
Sign	CLICK-CLICK Sign. 0: positive detection, 1: negative detection
Z	Z CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

7.20 CLICK_THS_A (3Ah)

Table 54. CLICK_THS_A register

--	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 55. CLICK_SRC_A description

Ths6-Ths0	CLICK-CLICK threshold. Default value: 000 0000

7.21 TIME_LIMIT_A (3Bh)

Table 56. TIME_LIMIT_A register

--	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 57. TIME_LIMIT_A description

TLI7-TLI0	CLICK-CLICK time limit. Default value: 000 0000

7.22 TIME_LATENCY_A (3Ch)

Table 58. TIME_LATENCY_A register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 59. TIME_LATENCY_A description

TLA7-TLA0	CLICK-CLICK time latency. Default value: 000 0000

7.23 TIME WINDOW_A (3Dh)

Table 60. TIME_WINDOW_A register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 61. TIME_WINDOW_A description

TW7-TW0	CLICK-CLICK time window

7.24 CTRL_REG1_G (20h)

Table 62. CTRL_REG1_G register

DR1	DR0	BW1	BW0	PD	Zen	0(1)	Xen

1. This bit must be set to ‘0’ for correct operation.

Table 63. CTRL_REG1_G description

DR1-DR0	Output data rate selection. Refer to *Table 64*
BW1-BW0	Bandwidth selection. Refer to *Table 64*
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used to set ODR selection. **BW <1:0>** is used to set Bandwidth selection.

Table 64 shows all frequencies resulting in combination of DR / BW bits.

Table 64. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-off
00	00	100	12.5
00	01	100	25
00	10	100	25
00	11	100	25
01	00	200	12.5
01	01	200	25
01	10	200	50
01	11	200	70
10	00	400	20
10	01	400	25
10	10	400	50
10	11	400	110
11	00	800	30
11	01	800	35
11	10	800	50
11	11	800	110

Combination of **PD, Zen, Xen** are used to set the device in different modes (power-down/normal/sleep mode) according to the following table.

Table 65. Power mode selection configuration

Mode	PD	Zen	Xen
Power-down	0	-	-
Sleep	1	0	0
Normal	1	-	-

7.25 CTRL_REG2_G (21h)

Table 66. CTRL_REG2_G register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. Value loaded at boot. This value must not be changed.

Table 67. CTRL_REG2_G description

HPM1-HPM0	High pass filter mode selection. Default value: 00 Refer to *Table 68*
HPCF3-HPCF0	High pass filter cut-off frequency selection Refer to *Table 69*

Table 68. High pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset an interrupt event

Table 69. High pass filter cut-off frequency configuration [Hz]

HPCF-0	ODR = 100 Hz	ODR = 200 Hz	ODR = 400 Hz	ODR = 800 Hz
0000	8	15	30	56
0001	4	8	15	30
0010	2	4	8	15
0011	1	2	4	8
0100	0.5	1	2	4
0101	0.2	0.5	1	2
0110	0.1	0.2	0.5	1
0111	0.05	0.1	0.2	0.5
1000	0.02	0.05	0.1	0.2
1001	0.01	0.02	0.05	0.1

7.26 CTRL_REG3_G (22h)

Table 70. CTRL_REG1_G register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 71. CTRL_REG3_G description

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)

Table 71. CTRL_REG3_G description (continued)

PP_OD	Push-pull/open drain. Default value: 0. (0: push-pull; 1: open drain)
I2_DRDY	Date ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

7.27 CTRL_REG4_G (23h)

Table 72. CTRL_REG4_G register

BDU	BLE	FS1	FS0	--	0(1)	0(1)	SIM

1. This bit must be set to '0' for correct operation.

Table 73. CTRL_REG4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

7.28 CTRL_REG5_G (24h)

Table 74. CTRL_REG5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 75. CTRL_REG5_G description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
HPen	High pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, see *Figure 12*)

Table 75. CTRL_REG5_G description (continued)

INT1_Sel1- INT1_Sel0	INT1 selection configuration. Default value: 0 (see *Table 77*)
Out_Sel1- Out_Sel0	Out selection configuration. Default value: 0 (see *Table 76*)

Figure 12. INT1_Sel and Out_Sel configuration block diagram

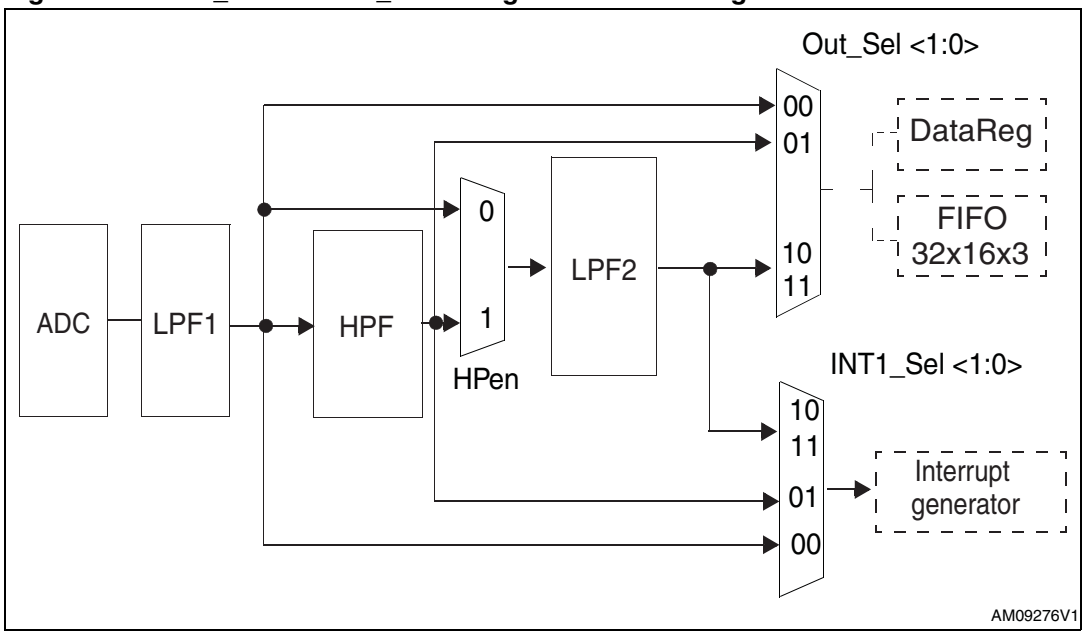


Table 76. Out_Sel configuration setting

Hpen	OUT_SEL1	OUT_SEL0	Description
x	0	0	Data in DataReg and FIFO are non-high-pass-filtered
x	0	1	Data in DataReg and FIFO are high-pass-filtered
0	1	x	Data in DataReg and FIFO are low-pass-filtered by LPF2
1	1	x	Data in DataReg and FIFO are high-pass and low-pass-filtered by LPF2

Table 77. INT_SEL configuration setting

Hpen	INT_SEL1	INT_SEL2	Description
x	0	0	Non-high-pass-filtered data are used for interrupt generation
x	0	1	High-pass-filtered data are used for interrupt generation

Table 77. INT_SEL configuration setting (continued)

Hpen	INT_SEL1	INT_SEL2	Description
0	1	x	Low-pass-filtered data are used for interrupt generation
1	1	x	High-pass and low-pass-filtered data are used for interrupt generation

7.29 REFERENCE/DATACAPTURE_G (25h)

Table 78. REFERENCE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 79. REFERENCE_G register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

7.30 OUT_TEMP_G (26h)

Table 80. OUT_TEMP_G register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 81. OUT_TEMP_G register description

Temp7-Temp0	Temperature data (1LSB/deg - 8 bit resolution). The value is expressed as two's complement.

7.31 STATUS_REG_G (27h)

Table 82. STATUS_REG_G register

ZXOR	ZOR	-	XOR	ZXDA	ZDA	--	XDA

Table 83. STATUS_REG_G description

ZXOR	X, Z-axis data overrun. Default value: 0 (0: no overrun has occurred, 1: new data has overwritten the previous one before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new data for the Z-axis has overwritten the previous one)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new data for the X-axis has overwritten the previous one)

Table 83. STATUS_REG_G description (continued)

ZXDA	X, Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
XDA	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

7.32 OUT_X_L_G (28h), OUT_X_H_G (29h)

X-axis angular rate data. The value is expressed as 2's complement.

7.33 OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)

Z-axis angular rate data. The value is expressed as 2's complement.

7.34 FIFO_CTRL_REG_G (2Eh)

Table 84. REFERENCE_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 85. REFERENCE_G register description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 86*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 86. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-stream mode

7.35 FIFO_SRC_REG_G (2Fh)

Table 87. FIFO_SRC_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 88. FIFO_SRC_G register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

7.36 INT1_CFG_G (30h)

Table 89. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	0(1)	0(1)	XHIE	XLIE

1. This bit must be set to ‘0’ for correct operation.

Table 90. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for interrupt source.

7.37 INT1_SRC_G (31h)

Table 91. INT1_SRC_G register

0	IA	ZH	ZL	--	--	XH	XL

Table 92. INT1_SRC_G description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: X low event has occurred)

Interrupt source register. Read only register.

Reading at this address clears the INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refreshment of data in the INT1_SRC register if the latched option is chosen.

7.38 INT1_THS_XH_G (32h)

Table 93. INT1_THS_XH_G register

--	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 94. INT1_THS_XH_G description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000

7.39 INT1_THS_XL_G (33h)

Table 95. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 96. INT1_THS_XL_G description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

7.40 INT1_THS_ZH_G (36h)

Table 97. INT1_THS_ZH_G register

--	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 98. INT1_THS_ZH_G description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000

7.41 INT1_THS_ZL_G (37h)

Table 99. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 100. INT1_THS_ZL_G description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

7.42 INT1_DURATION_G (38h)

Table 101. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 102. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

WAIT bit has the following meaning:

Wait ='0': the interrupt falls immediately if signal crosses the selected threshold

Wait ='1': if signal crosses the selected threshold, the interrupt falls only after the duration has counted a number of samples at the selected data rate, written into the duration counter register.

Figure 13. Wait disabled

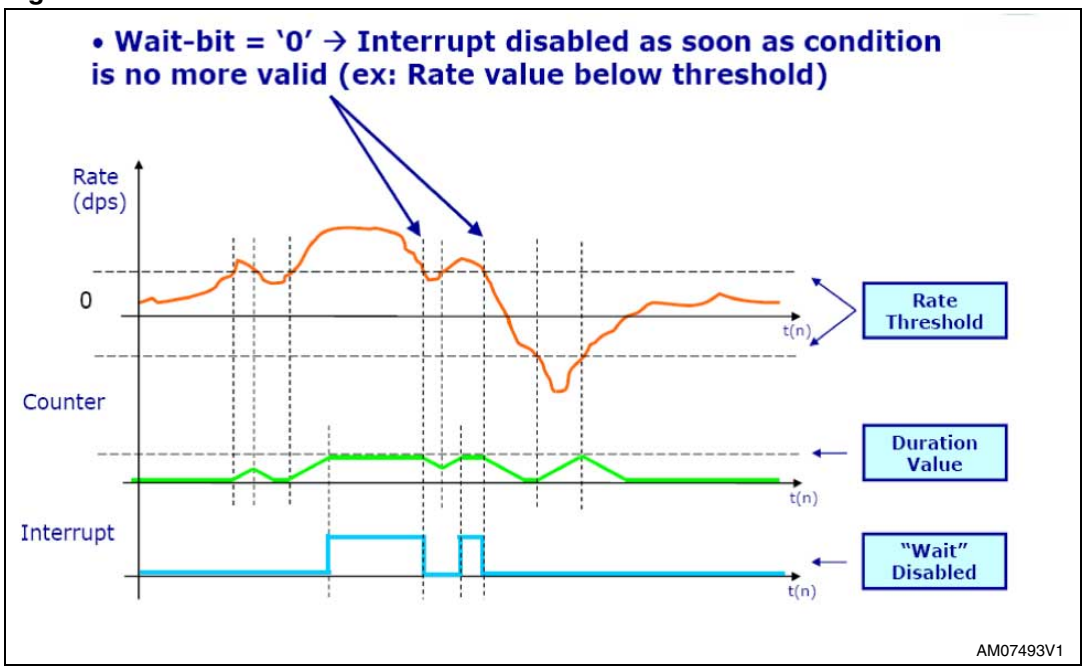
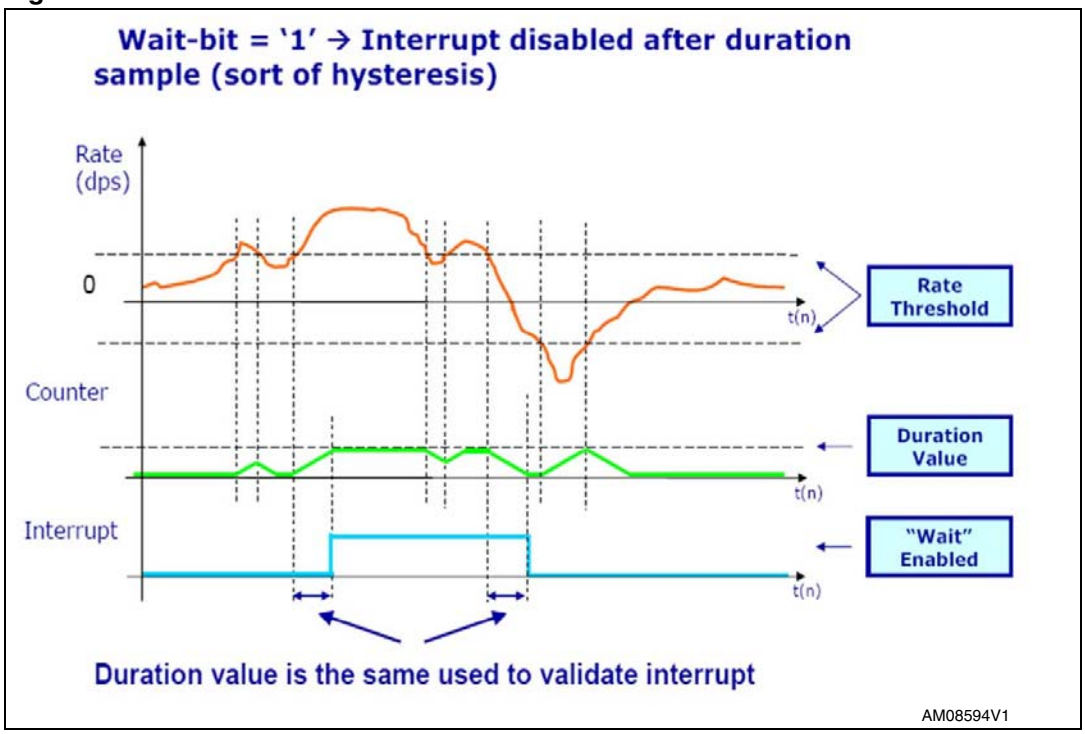


Figure 14. Wait enabled



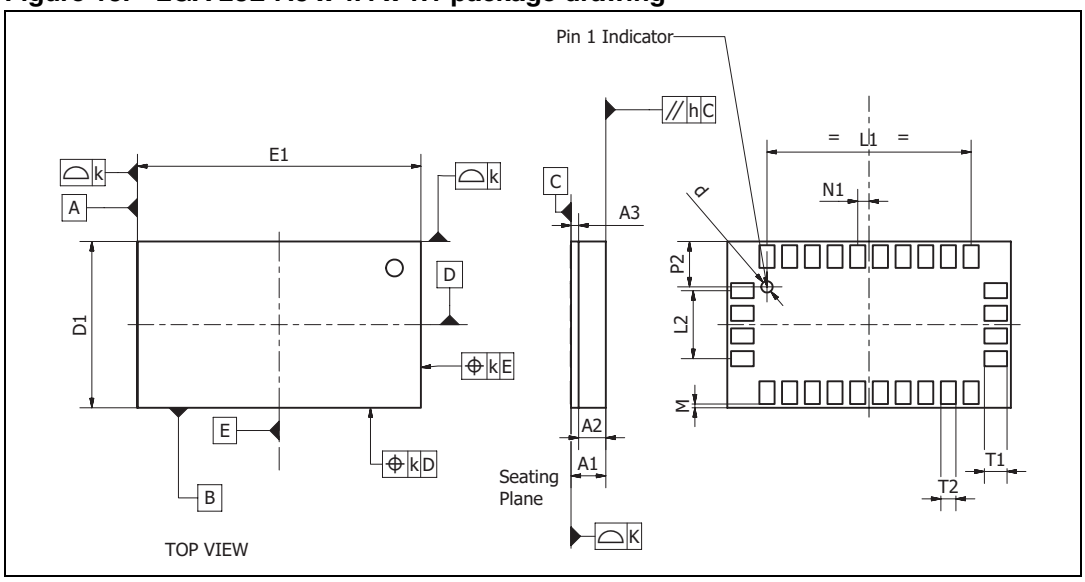
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com.
ECOPACK is an ST trademark.

Table 103. LGA 28L 7.5 x 4.4 x 1.1 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1.1
A2		0.855	
A3		0.2	
D1	4.25	4.4	4.55
E1	7.25	7.5	7.55
N1		0.3	
L1		5.4	
L2		1.8	
P2		1.2	
T1		0.6	
T2		0.4	
M		0.1	
d		0.3	
k		0.05	
h		0.1	

Figure 15. LGA 28L 7.5 x 4.4 x 1.1 package drawing



9 Revision history

Table 104. Document revision history

Date	Revision	Changes
18-May-2011	1	Initial release.

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